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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MN

Office Action Summary	Application No.	Applicant(s)	
	10/643,741	SCOTT ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-14 and 19-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-14 and 19-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/4/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed June 6, 2007 in response to the Office action dated May 5, 2007. Claims 1-5, 9-14, and 19-23 have been amended. Claims 7-8, and 15-18 have been canceled. New claims 24-29 have been added. Claims 1-6, 9-14, and 19-29 are pending in this application.

OBJECTIONS

Drawings

1. In view of Applicant's amendments, the objection to the drawings has been withdrawn.

Claims

2. In view of Applicant's amendments, the objection to **claims 19 and 22** have been withdrawn.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

3. In view of Applicant's amendments, the 112 rejections to **claims 1-23** have been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 11, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith et al. (U.S. Patent Application Publication 2002/0116600) (hereinafter "Smith").

6. **As per claim 1**, Smith discloses an apparatus comprising:

a memory interface (Fig. 6A, the interface for element 162);

a plurality of queues connected to the memory interface, including a first queue and a second queue, each of the first plurality of queues for holding a plurality of pending memory requests (paragraph 0077; Fig. 6A); *It should be noted that thread 0 within the reorder buffer is analogous to the "first queue" and thread 1 within the reorder buffer is analogous to the "second queue." It should also be noted that the "microinstructions" are analogous to "memory requests."*

one or more instruction-processing circuits, wherein each instruction-processing circuit is operatively coupled through the plurality of queues to the memory interface and wherein each of the plurality of instruction-processing circuits inserts one or more memory requests into at least one of the queues based on a first memory operation instruction, inserts a first synchronization marker into the first queue and inserts a second synchronization marker into the second queue based on a synchronization

operation instruction and inserts one or more memory requests into at least one of the queues based on a second memory operation instruction (paragraph 0039; paragraph 0077; paragraph 0100; Fig. 2, elements 42 and 66); *It should be noted that the "microcode sequencer" and "microinstruction translation engine" are analogous to "instruction-processing circuits" and the "macroinstructions" are analogous to the "memory operation and synchronization operation instructions."*

and a first synchronization circuit, operatively coupled to the first plurality of queues, that selectively halts processing of further memory requests from the first queue based on the first synchronization marker reaching a predetermined point in the first queue until the corresponding second synchronization marker reaches a predetermined point in the second queue (paragraph 0100; paragraph 0103; paragraph 0109; Fig. 6A, element 188; Fig. 7A, elements 222, 270, and 288); *It should be noted that the "event handler" is analogous to the "synchronization circuit."*

wherein each of the memory requests is a memory reference, wherein the memory reference is generated as a result of instructions by the instruction-processing circuits (paragraph 0039). *It should be noted that the microinstruction translation engine translates (i.e. decodes and executes) a macroinstruction into a corresponding microinstruction. Thus, the memory macroinstructions being executed would in turn generate the memory microinstructions (i.e. memory references).*

7. **As per claim 11**, Smith discloses a method comprising:

providing a memory interface (Fig. 6A, the interface for element 162);

providing a plurality of queues connected to the memory interface, including a first queue and a second queue, each of the first plurality of queues for holding a plurality of pending memory requests (paragraph 0077; Fig. 6A);

providing one or more instruction-processing circuits, wherein each instruction-processing circuit is operatively coupled through the plurality of queues to the memory interface (paragraph 0039; paragraph 0100; Fig. 2, elements 42 and 66); *See the citation note for the similar limitation in claim 1 above.*

inserting one or more memory requests into at least one of the queues based on a first memory operation instruction executed in one of the instruction-processing circuits (paragraph 0039; paragraph 0077; Fig. 2, element 42); *See the citation note for the similar limitation in claim 1 above. Also, it should be noted that the microinstruction translation engine translates (i.e. executes) a macroinstruction into a corresponding microinstruction.*

inserting a first synchronization marker into the first queue and inserting a second synchronization marker into the second queue based on a synchronization operation instruction executed in one of the instruction-processing circuits (paragraph 0039; paragraph 0100; Fig. 2, elements 42 and 66); *See the citation note for the limitation directly above.*

inserting one or more memory requests into at least one of the queues based on a second memory operation instruction based on a second memory operation instruction executed in one of the instruction-processing circuits (paragraph 0039;

paragraph 0077; Fig. 2, element 42); *See the citation note for the limitation directly above.*

processing memory requests from the first queue (paragraph 0079; Fig. 2, element 70);

and selectively halting further processing of memory requests from the first queue based on the first synchronization marker reaching a predetermined point in the first queue until the corresponding second synchronization marker reaches a predetermined point in the second queue (paragraph 0100; paragraph 0103; paragraph 0109; Fig. 6A, element 188; Fig. 7A, elements 222, 270, and 288).

wherein each of the memory requests is a memory reference (paragraph 0039). *See the citation note for the last limitation in claim 1 above.*

8. **As per claim 21**, Smith discloses an apparatus comprising:

a memory interface (Fig. 6A, the interface for element 162);

a plurality of queues connected to the memory interface, including a first queue and a second queue, each of the first plurality of queues for holding a plurality of pending memory requests (paragraph 0077; Fig. 6A); *See the citation note for the similar limitation in claim 1 above.*

one or more instruction-processing circuits, wherein each instruction-processing circuit is operatively coupled through the plurality of queues to the memory interface (paragraph 0039; paragraph 0100; Fig. 2, elements 42 and 66); *See the citation note for the similar limitation in claim 1 above.*

and wherein each of the plurality of instruction-processing circuits includes:

means for inserting one or more memory requests into at least one of the queues based on a first memory operation instruction executed in one of the instruction-processing circuits (paragraph 0039; paragraph 0077; Fig. 2, element 42); *See the citation note for the similar limitation in claim 11 above.*

means for inserting a first synchronization marker into the first queue and inserting a second synchronization marker into the second queue based on a synchronization operation instruction executed in one of the instruction-processing circuits (paragraph 0039; paragraph 0100; Fig. 2, elements 42 and 66); *See the citation note for the similar limitation in claim 11 above.*

means for inserting one or more memory requests into at least one of the queues based on a second memory operation instruction based on a second memory operation instruction executed in one of the instruction-processing circuits (paragraph 0039; paragraph 0077; Fig. 2, element 42); *See the citation note for the similar limitation in claim 11 above.*

means for processing memory requests from the first queue (paragraph 0079; Fig. 2, element 70);

and means for selectively halting further processing of memory requests from the first queue based on the first synchronization marker reaching a predetermined point in the first queue until the corresponding second synchronization marker reaches a predetermined point in the second queue (paragraph 0100; paragraph 0103; paragraph 0109; Fig. 6A, element 188; Fig. 7A, elements 222, 270, and 288).

wherein each of the memory requests is a memory reference (paragraph 0039).

See the citation note for the last limitation in claim 1 above.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2, 5, 9, 12, 19, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Chen et al. (U.S. Patent 5,197,130) (hereinafter "Chen").

11. **As per claims 2 and 12**, Smith discloses the first queue is used for only synchronization markers and memory references, and the second queue is used for only synchronization markers and memory references (paragraph 0039; paragraph 0077; paragraph 0100).

Smith does not expressly disclose the memory references are vectors memory references and scalar memory references respectively.

Chen discloses the first queue is used only for vector memory references and the second queue is used only for scalar memory references (col. 10, line 65 – col. 11, line 17; Fig. 4).

Smith and Chen are analogous art because they are from the same field of endeavor, that being processor systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Chen's vector and scalar processing means with Smith's multithreaded processor to create a multiprocessor cluster.

The motivation for doing so would have been to increase system performance by providing a multiprocessor cluster of tightly-coupled, high-speed processors capable of both vector and scalar parallel processing that can symmetrically access shared resources (Chen, col. 6, line 65 – col. 7, line 1).

Therefore, it would have been obvious to combine Smith and Chen for the benefit of obtaining the invention as specified in claims 2 and 12.

12. **As per claim 5**, the combination of Smith/Chen discloses for a second synchronization operation instruction, a corresponding synchronization marker is inserted in only the first queue (Smith, paragraph 0100; paragraph 0104; Fig. 7A, element 272).

13. **As per claims 9 and 19**, the combination of Smith/Chen discloses the first queue includes two subqueues, including a first subqueue and a second subqueue, wherein the first subqueue is for holding the vector memory references and synchronization markers associated with the vector memory references (Smith, paragraph 0039; paragraph 0077; paragraph 0100; Chen, col. 10, line 65 – col. 11, line 17) and wherein the second subqueue is for holding a plurality of store data elements and synchronization markers associated with the store data elements, wherein each store data element in the second subqueue corresponds to one of the memory requests in the first subqueue, and wherein the store data elements are loaded into the second

subqueue decoupled from the loading of the memory requests into the first subqueue (Smith, paragraph 0039; paragraph 0077; paragraph 0100; Chen, col. 17, lines 55-58; col. 18, lines 13-30; Fig. 14, element 326).

14. **As per claim 22**, Smith discloses means for inserting to the first queue operates for only memory requests and synchronizations, and means for inserting to the second queue operates for only memory requests and synchronizations (paragraph 0039; paragraph 0077; paragraph 0100).

Smith does not expressly disclose the memory requests are vectors memory requests and scalar memory requests respectively.

Chen discloses means for inserting to the first queue operates for only vector memory requests and means for inserting to the second queue operates for only scalar memory requests (col. 10, line 65 – col. 11, line 17; Fig. 4).

Please see the 103 rejection of claims 2 and 12 above (Smith in view of Chen) for the reasons to combine Smith and Chen.

15. Claims 3-4, 6, 10, 13-14, 20, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Chen, as applied to claims 2, 12, and 22 above, and further in view of "Cray Assembly Language (CAL) for Cray X1 System Reference Manual" (hereinafter "Cray").

16. **As per claims 3, 13, and 23**, the combination of Smith/Chen discloses all the limitations of claim 3 except the synchronization operation instruction is an Lsync-type instruction.

Cray discloses the synchronization operation instruction is an Lsync-type instruction (Section 2.6, Table 17, rows 8-15).

The combination of Smith/Chen and Cray are analogous art because they are from the same field of endeavor, that being computer processing systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Cray's Lsync-type instructions within Smith/Chen's multiprocessor cluster because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of explicit memory ordering via the synchronization instructions.

Therefore, it would have been obvious to combine Smith/Chen and Cray for the benefit of obtaining the invention as specified in claims 3, 13, and 23.

17. **As per claims 4 and 14**, the combination of Smith/Chen/Cray discloses the synchronization operation instruction is an Lsync V,S-type instruction (Cray, Section 2.6, Table 17, row 9).

18. **As per claim 6**, the combination of Smith/Chen/Cray discloses the second synchronization operation instruction is an Lsync-type instruction (Cray, Section 2.6, Table 17, rows 8-15).

19. **As per claims 10 and 20**, the combination of Smith/Chen/Cray discloses the instruction-processing circuits include a data cache and wherein the Lsync V,S-type instruction prevents subsequent scalar references from accessing the data cache until all vector references have been sent to an external cache and all vector writes have

caused any necessary invalidations of the data cache (Cray, Section 2.6, Table 17, row 9; Smith, Fig. 2, element 44).

20. Claims 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Barnes et al. (U.S. Patent 4,412,303) (hereinafter "Barnes) and Cray.

21. **As per claim 24**, Smith discloses a system comprising:

a first processor (Fig. 2), wherein the processor includes:

a memory interface (Fig. 6A, the interface for element 162);

a plurality of queues connected to the memory interface, including a first queue and a second queue, each of the first plurality of queues for holding a plurality of pending memory requests (paragraph 0077; Fig. 6A); *See the citation note for the similar limitation in claim 1 above.*

one or more instruction-processing circuits, wherein each instruction-processing circuit is operatively coupled through the plurality of queues to the memory interface and wherein each of the plurality of instruction-processing circuits inserts one or more memory requests into at least one of the queues based on a first memory operation instruction, inserts a first synchronization marker into the first queue and inserts a second synchronization marker into the second queue based on a synchronization operation instruction and inserts one or more memory requests into at least one of the queues based on a second memory operation instruction (paragraph 0039; paragraph 0077; paragraph 0100; Fig. 2, elements 42 and 66); *See the citation note for the similar limitation in claim 1 above.*

and a first synchronization circuit, operatively coupled to the first plurality of queues, that selectively halts processing of further memory requests from the first queue based on the first synchronization marker reaching a predetermined point in the first queue until the corresponding second synchronization marker reaches a predetermined point in the second queue (paragraph 0100; paragraph 0103; paragraph 0109; Fig. 6A, element 188; Fig. 7A, elements 222, 270, and 288); *See the citation note for the similar limitation in claim 1 above.*

wherein each of the memory requests is a memory reference, wherein the memory reference is generated as a result of instructions by the instruction-processing circuits (paragraph 0039). *See the citation note for the similar limitation in claim 1 above.*

Smith does not expressly disclose using Lsync instructions as well as one or more Msync circuits, wherein each of the Msync circuits is connected to the plurality of processors and wherein each of the Msync circuits includes:

a plurality of Msync queues, including a first Msync queue and a second Msync queue, each of the plurality of Msync queues for holding a plurality of pending memory requests received from the Lsync queues, wherein the first Msync queue stores only Msync synchronization markers and memory requests from the first processor, and the second Msync queue stores only Msync synchronization markers and memory requests from the second processor; and

an Msync synchronization circuit, operatively coupled to the plurality of Msync queues, that selectively halts further processing of the memory requests from the first

Msync queue based on an Msync synchronization marker reaching a predetermined point in the first Msync queue until a corresponding Msync synchronization marker from the second processor reaches a predetermined point in the second Msync queue.

Barnes discloses a second plurality of queues, including a third queue and a fourth queue, each of the second plurality of queues for holding a plurality of pending memory requests received from the first plurality of queues; wherein the third queue stores only synchronization markers and memory requests the first processor, and the second queue stores only synchronization markers and memory requests from the second processor (col. 5, lines 50-55; col. 6, lines 4-31 and 39-55; Fig. 1, elements 23 and 29). *It should be noted that the "proc. 0" analogous to the "first processor", "proc. 1" is analogous to the "second processor", the "connection network buffer" within proc. 0 is analogous to the "third queue", and the "connection network buffer" within proc. 1 is analogous to the "fourth queue."*

a second synchronization circuit, operatively coupled to the second plurality of queues, that selectively halts further processing of memory requests from the third queue based on the first synchronization marker reaching a predetermined point in the third queue until a corresponding synchronization marker from the second processor reaches a predetermined point in the fourth queue (Barnes, col. 7, lines 28-47; Fig. 3, element 21). *It should be noted that the "coordinator" is analogous to the "second synchronization circuit."*

Smith and Barnes are analogous art because they are from the same field of endeavor, that being processor systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Barnes' queues and synchronization circuits with Smith's queues and synchronization circuits.

The motivation for doing so would have been to efficiently process vector and other data elements in a parallel but not a locked-step fashion (Barnes, col. 2, lines 48-50).

The combination of Smith/Barnes does not expressly disclose using Lsync instructions and Msync instructions.

Cray discloses using Lsync instructions and Msync instructions (Section 2.6, Table 17, rows 5-15).

The combination of Smith/Chen and Cray are analogous art because they are from the same field of endeavor, that being computer processing systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Cray's Lsync instructions within Smith's queues and synchronization circuits and Cray's Msync instructions within Barnes' queues and synchronization circuits because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of explicit memory ordering via the synchronization instructions.

Therefore, it would have been obvious to combine Smith, Barnes, and Cray for the benefit of obtaining the invention as specified in claim 24.

22. **As per claim 25**, the combination of Smith/Barnes/Cray discloses the Msync synchronization circuit includes a plurality of stall lines, wherein each of the stall lines is connected to one of the plurality of Msync queues and wherein each of the stall lines is for halting further processing of the memory requests for a corresponding Msync queue (Barnes, col. 7, lines 28-47; Fig. 3, element 21; Cray, Section 2.6, Table 20, rows 5-7). *It should be noted that it is required there be some sort of "stall lines" in the circuitry in order to halt processing of memory requests in the queue.*

23. **As per claim 26**, the combination of Smith/Chen/Cray discloses each processor includes a data cache and wherein each Msync synchronization circuit includes and external cache, wherein the data cache and external cache are sued to perform an Lsync V,S-type instruction, wherein the Lsync V,S-type instruction prevents subsequent scalar references from accessing the data cache until all vector references have been sent to the external cache in a corresponding Msync synchronization circuit and all vector writes have caused any necessary invalidations of the data cache (Cray, Section 2.6, Table 17, row 9; Smith, Fig. 2, element 44).

24. **As per claim 27**, Smith discloses a method comprising:

a first processor (Fig. 2), wherein the processor includes a memory interface (Fig. 6A, the interface for element 162), a plurality of queues connected to the memory interface, including a first queue and a second queue, each of the first plurality of queues for holding a plurality of pending memory requests (paragraph 0077; Fig. 6A), and one or more instruction-processing circuits, wherein each instruction-processing circuit is operatively coupled through the plurality of queues to the memory interface

(paragraph 0039; paragraph 0100; Fig. 2, elements 42 and 66); *See the citation note for the similar limitation in claim 1 above.*

inserting one or more memory requests into at least one of the queues based on a first memory operation instruction executed in one of the instruction-processing circuits (paragraph 0039; paragraph 0077; Fig. 2, element 42); *See the citation note for the similar limitation in claim 1 above. Also, it should be noted that the microinstruction translation engine translates (i.e. executes) a macroinstruction into a corresponding microinstruction.*

inserting a first synchronization marker into the first queue and inserting a second synchronization marker into the second queue based on a synchronization operation instruction executed in one of the instruction-processing circuits (paragraph 0039; paragraph 0100; Fig. 2, elements 42 and 66); *See the citation note for the limitation directly above.*

inserting one or more memory requests into at least one of the queues based on a second memory operation instruction based on a second memory operation instruction executed in one of the instruction-processing circuits (paragraph 0039; paragraph 0077; Fig. 2, element 42); *See the citation note for the limitation directly above.*

processing memory requests from the first queue (paragraph 0079; Fig. 2, element 70);

and selectively halting further processing of memory requests from the first queue based on the first synchronization marker reaching a predetermined point in the

first queue until the corresponding second synchronization marker reaches a predetermined point in the second queue (paragraph 0100; paragraph 0103; paragraph 0109; Fig. 6A, element 188; Fig. 7A, elements 222, 270, and 288).

wherein each of the memory requests is a memory reference (paragraph 0039). *See the citation note for the last limitation in claim 1 above.*

Smith does not expressly disclose using Lsync instructions as well as providing one or more Msync circuits, wherein each of the Msync circuits is connected to the plurality of processors and wherein each of the Msync circuits includes a plurality of Msync queues, including a first Msync queue and a second Msync queue, each of the plurality of Msync queues operatively coupled to the plurality of Lsync queues in one of the plurality of processors;

inserting Msync synchronization markers and memory requests received from the Lsync queues in the first processor into the first Msync queue;

inserting Msync synchronization markers and memory requests received from the Lsync queues in the second processor into the second Msync queue; and

selectively halting further processing of the memory requests from the first Msync queue based on an Msync synchronization marker reaching a predetermined point in the first Msync queue until a corresponding Msync synchronization marker from the second processor reaches a predetermined point in the second Msync queue.

Barnes discloses providing one or more circuits, wherein each of the circuits is connected to the plurality of processors and wherein each of the circuits includes a plurality of queues, including a third queue and a fourth queue, each of the plurality of

queues operatively coupled to the first plurality of queues in one of the plurality of processors (col. 5, lines 50-55; col. 6, lines 4-31 and 39-55; Fig. 1, elements 23 and 29); *See the citation note for the similar limitation in claim 24 above.*

inserting synchronization markers and memory requests received from the first plurality of queues in the first processor into the third queue (col. 6, lines 4-31 and 39-55);

inserting synchronization markers and memory requests received from the first plurality of queues in the second processor into the fourth queue (col. 6, lines 4-31 and 39-55).

and selectively halting further processing of the memory requests from the third queue based on a synchronization marker reaching a predetermined point in the third queue until a corresponding synchronization marker from the second processor reaches a predetermined point in the fourth queue (col. 7, lines 28-47; Fig. 3, element 21).

Smith and Barnes are analogous art because they are from the same field of endeavor, that being processor systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Barnes' queues and synchronization circuits with Smith's queues and synchronization circuits.

The motivation for doing so would have been to efficiently process vector and other data elements in a parallel but not a locked-step fashion (Barnes, col. 2, lines 48-50).

The combination of Smith/Barnes does not expressly disclose using Lsync instructions and Msync instructions.

Cray discloses using Lsync instructions and Msync instructions (Section 2.6, Table 17, rows 5-15).

The combination of Smith/Chen and Cray are analogous art because they are from the same field of endeavor, that being computer processing systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Cray's Lsync instructions within Smith's queues and synchronization circuits and Cray's Msync instructions within Barnes' queues and synchronization circuits because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of explicit memory ordering via the synchronization instructions.

Therefore, it would have been obvious to combine Smith, Barnes, and Cray for the benefit of obtaining the invention as specified in claim 27.

25. **As per claim 28**, the combination of Smith/Barnes/Cray discloses selectively halting further processing of the memory requests from the first Msync queue includes sending a stall signal to the Msync queues (Barnes, col. 7, lines 28-47; Fig. 3, element 21; Cray, Section 2.6, Table 20, rows 5-7). *See the citation note for claim 25 above.*

26. **As per claim 29**, the combination of Smith/Chen/Cray discloses selectively halting further processing of memory requests from the first Lsync queue includes

performing an Lsync V,S type instruction, wherein performing the Lsync V,S type instruction includes preventing subsequent scalar references from accessing a data cache in the processor until all vector references have been sent to an external cache in a corresponding Msync synchronization circuit and all vector writes have caused any necessary invalidations of the data cache (Cray, Section 2.6, Table 17, row 9; Smith, Fig. 2, element 44).

Response to Arguments

27. Applicant's arguments filed June 4, 2007 with respect to claims **1-6, 9-14, and 19-29** have been fully considered but they are not persuasive.

28. With respect to Applicant's argument in the second full paragraph on page 13 of the communication filed June 4, 2007 regarding a memory interface, the Examiner respectfully disagrees. It is clear that a buffer is a type of memory. It is also clear that any memory inherently has at least one interface in order to properly connect to and interact with external devices. As can be seen in Figs. 2 and 6A of Smith the reorder buffer (which contains threads 0 and 1) interfaces with the front of the microprocessor. Taking these facts into consideration, the Examiner submits that the reorder buffer's interface with the front of the microprocessor sufficiently discloses Applicant's "memory interface" as simply and broadly claimed.

29. With respect to Applicant's argument in the third full paragraph on page 13 of the communication filed June 4, 2007, the Examiner respectfully disagrees. As can be seen in the last 3 lines of paragraph 0039 of Smith, microinstruction translation engine

54 translates (i.e. decodes and executes) the macroinstructions into a corresponding set of microinstructions. Thus, the microinstructions regarding memory transactions are generated as a result of the execution of macroinstructions regarding memory transactions by the microinstruction translation engine. Accordingly, Smith sufficiently discloses each of the memory requests is a memory reference, wherein the memory reference is generated as a result of instructions by the instruction-processing circuits.

30. With respect to Applicant's argument in the fifth and sixth full paragraphs on page 14 of the communication filed June 4, 2007, the Examiner respectfully disagrees. It is noted that the features upon which Applicant relies (i.e., "controlling the order in which the resulting memory references are processed into a memory") are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Claims 2, 12, and 22 merely recite that the first queue is used for only synchronization markers and vector memory references, and the second queue is used for only synchronization markers and scalar memory references. Nowhere in the claim language does it recite anything about controlling the order in which the resulting memory references are processed into a memory. Accordingly, the combination of Smith and Chen sufficiently discloses the language of claims 2, 12, and 22.

31. With respect to Applicant's argument in the second full paragraph on page 15 of the communication filed June 4, 2007, the argument is moot in view of the new grounds of rejection above.

32. As for Applicant's arguments with respect to the dependent claims, the arguments rely on the allegation that the independent claims are allowable and therefore for the same reasons the dependent claims are allowable. However, as addressed above, the independent claims are not allowable, thus, Applicant's arguments with respect to the dependent claims are not persuasive.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-6, 9-14, and 19-29** have received a second action on the merits and are subject of a second action final.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
Art Unit 2185
September 3, 2007

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